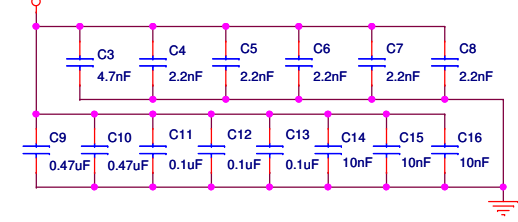


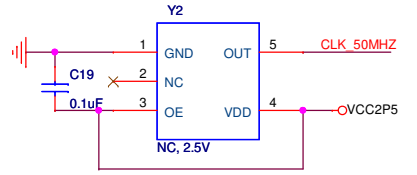
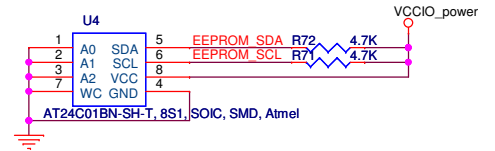
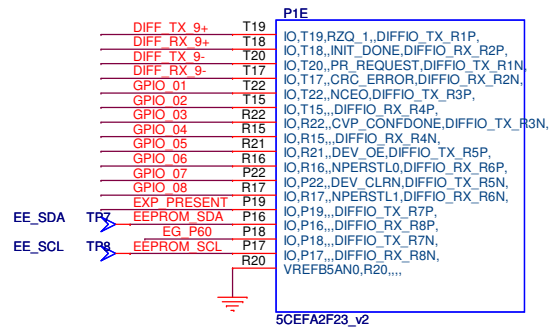
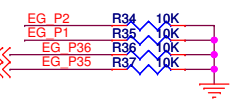
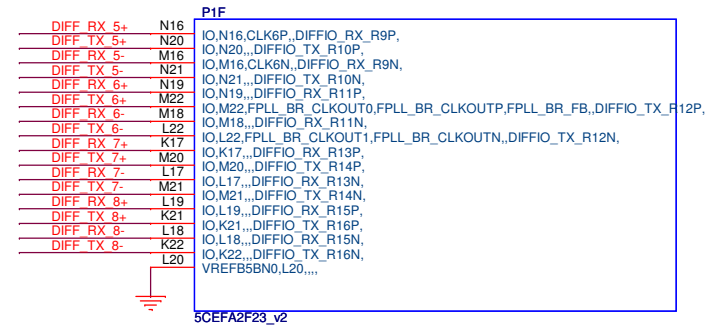
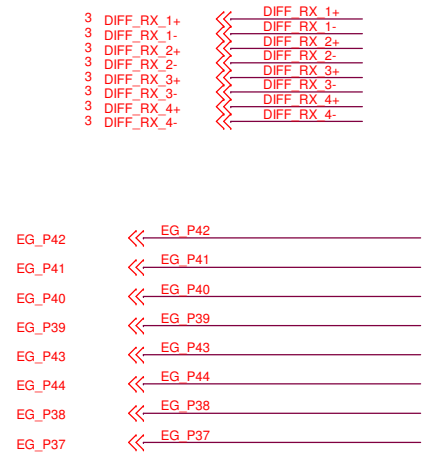
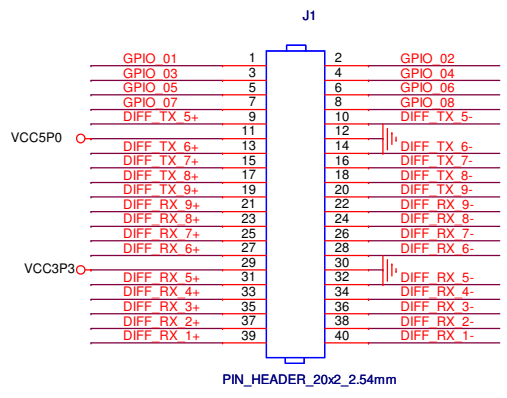
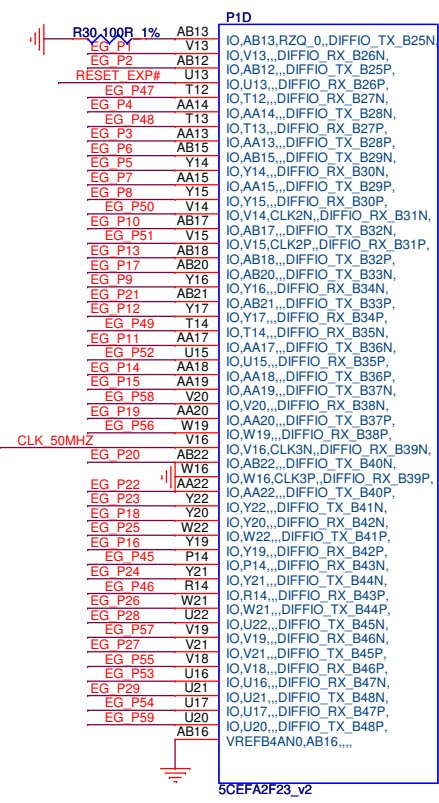
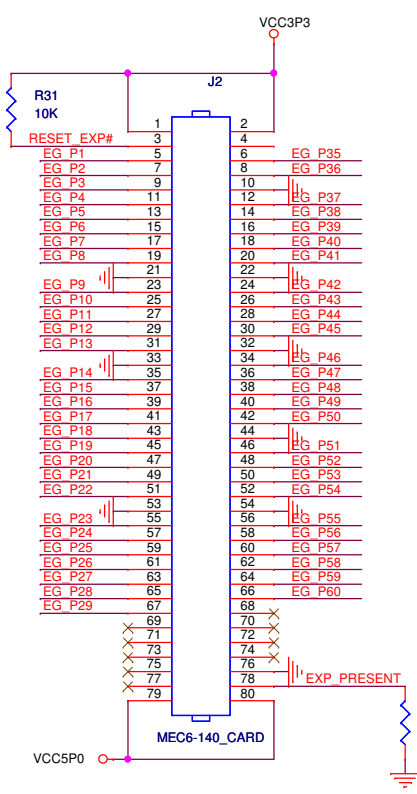
CAD Note:
Place cap arrays near resistor packs and on the same side of PCB

CAD Note:
Use tree-topology for termination signals
Use star via to branch out address/command/control signals from FPGA to memory devices and termination resistors

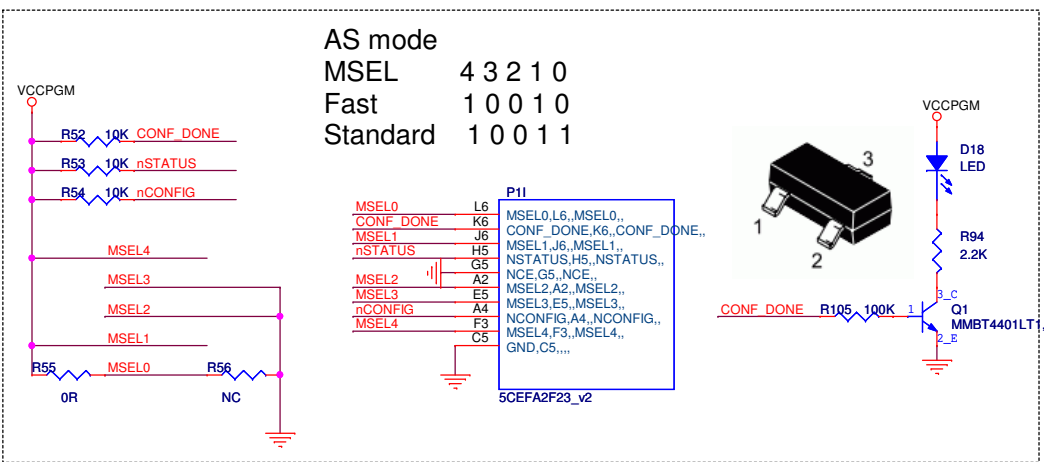
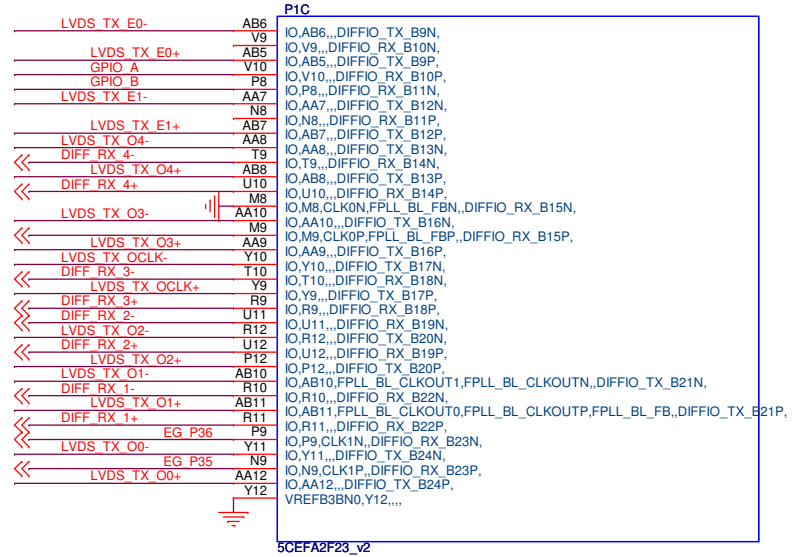
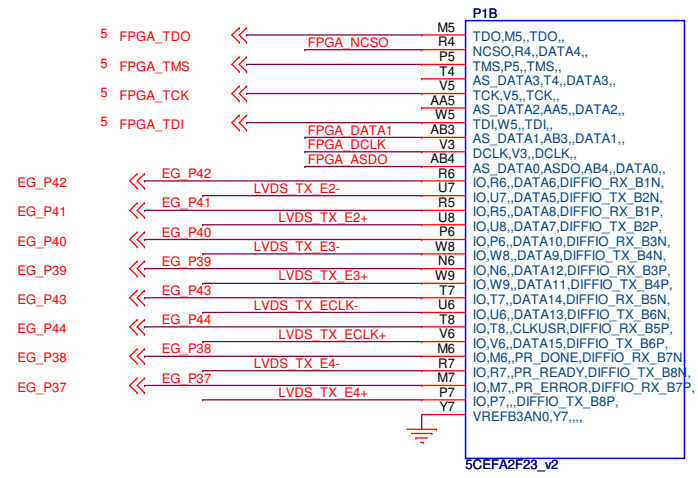
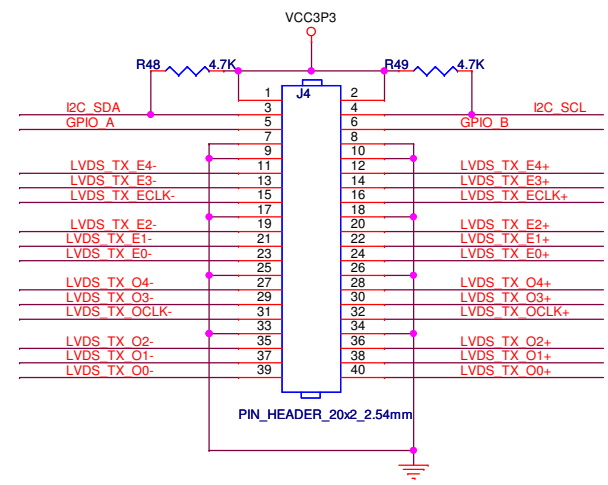
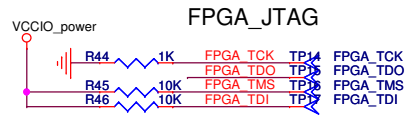
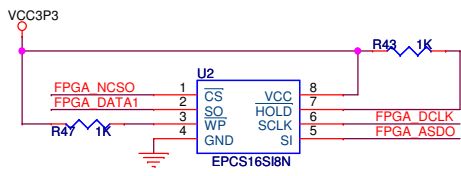
CAD Note:
Place decoupling caps near SDRAM power pins



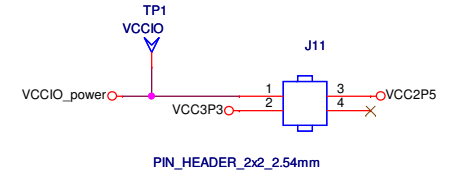
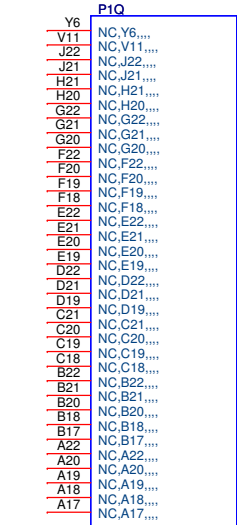
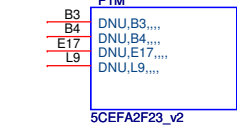
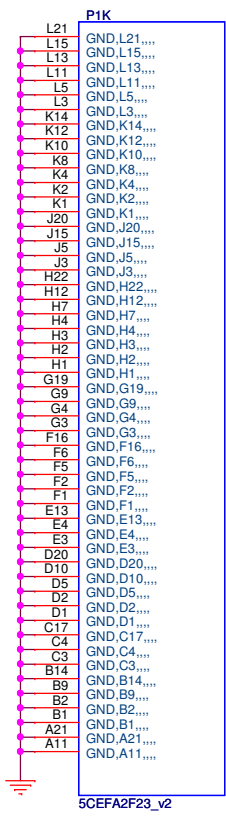
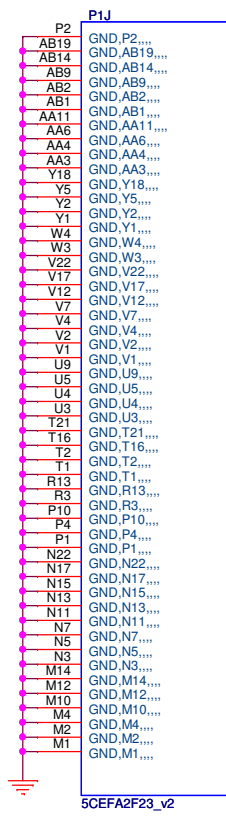
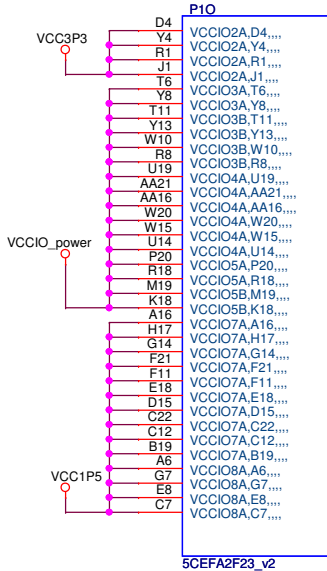
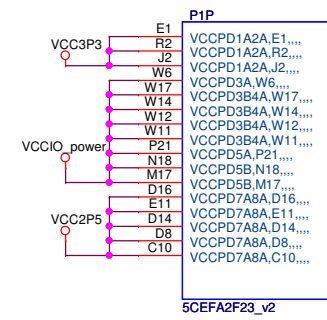
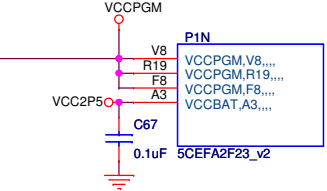
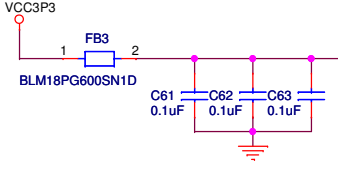
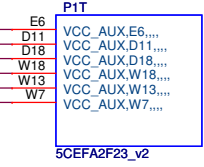
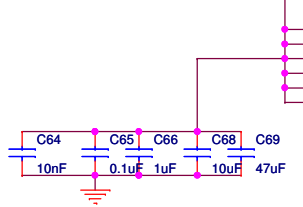
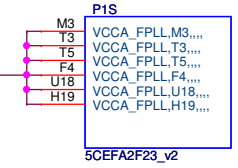
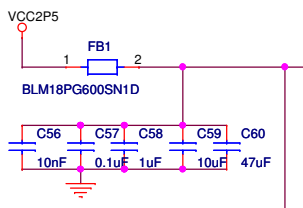
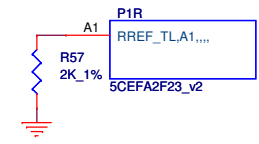
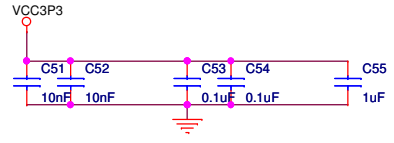
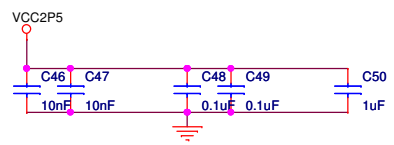
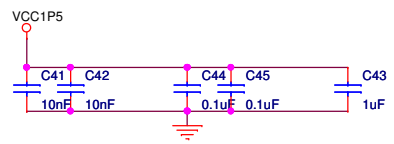
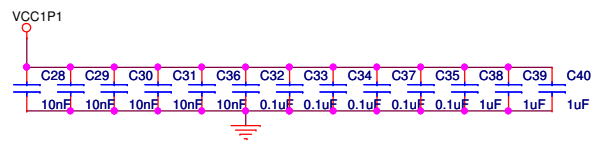
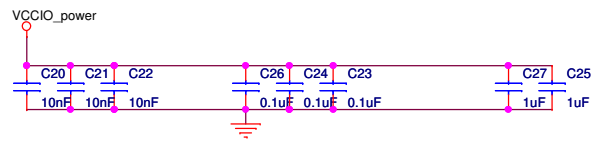
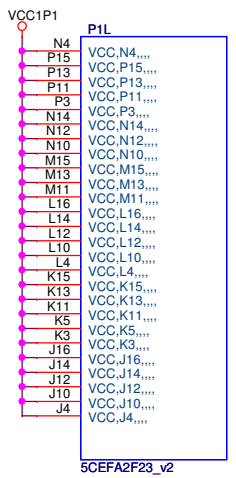
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Size	Document Number	Rev
B	DDR3	<RevCode>
Date:	Wednesday, May 15, 2013	Sheet 1 of 7



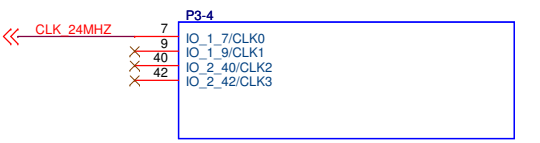
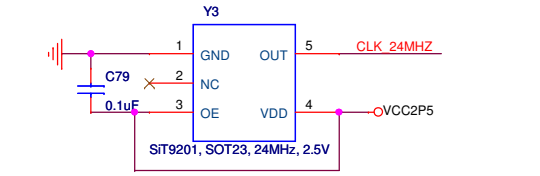
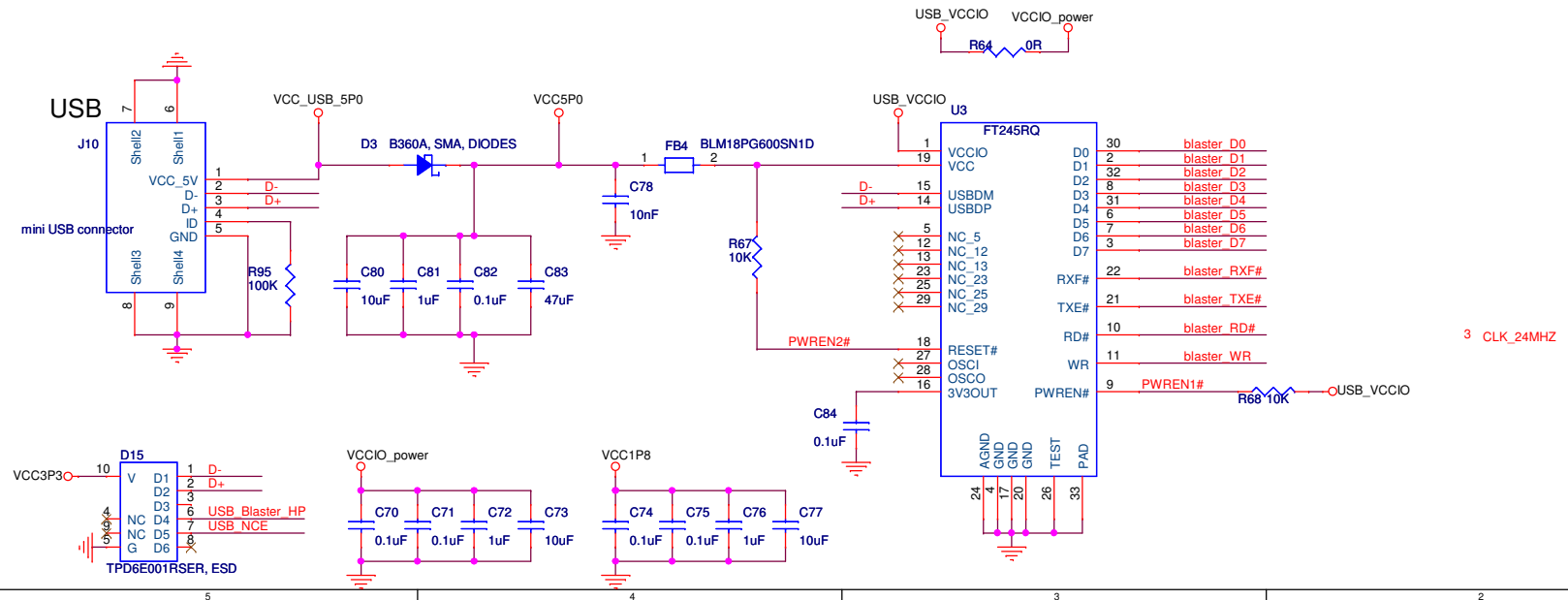
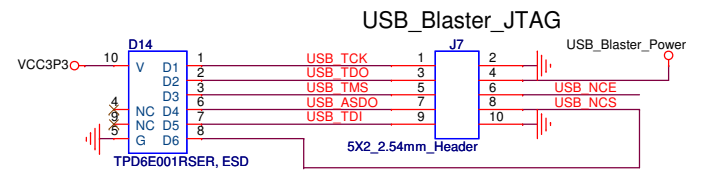
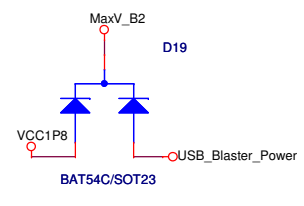
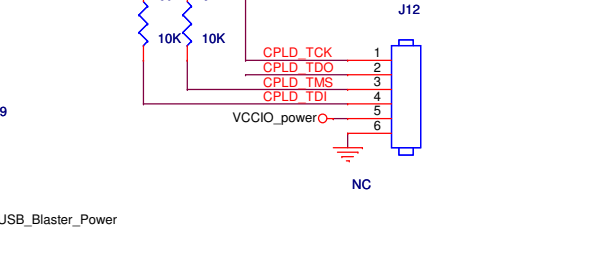
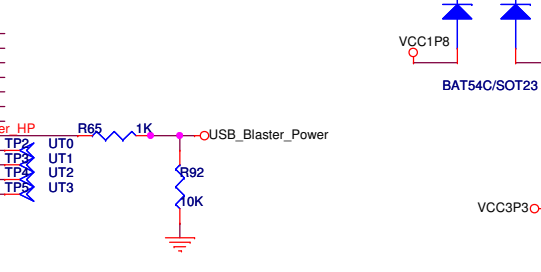
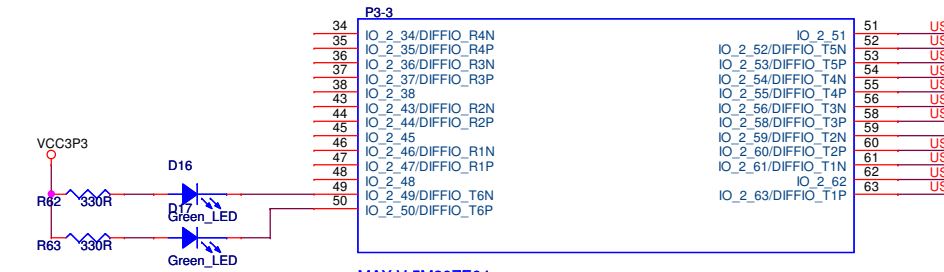
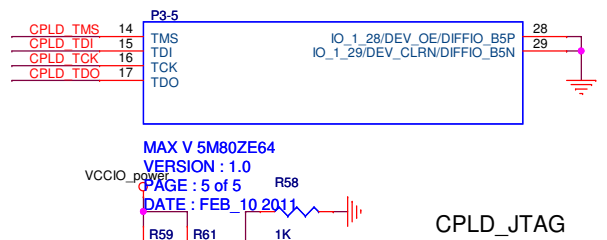
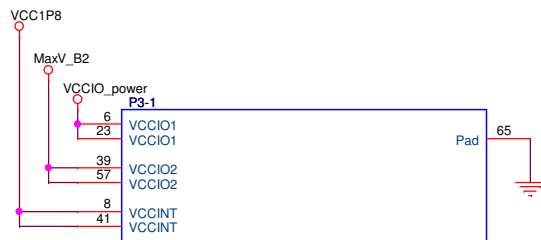
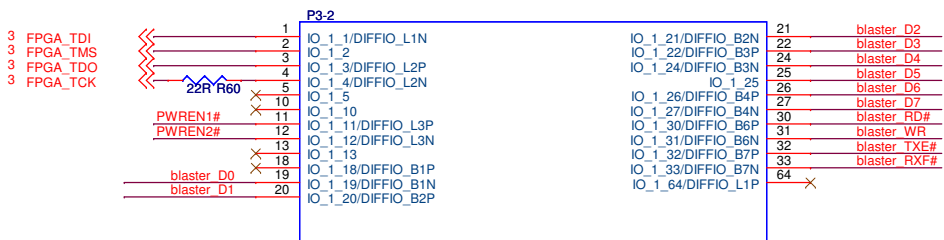
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B	80-pin Edge Connector, uSD Card, 20x2 pin header	<RevCode>
Date:	Monday, May 06, 2013	Sheet 2 of 7



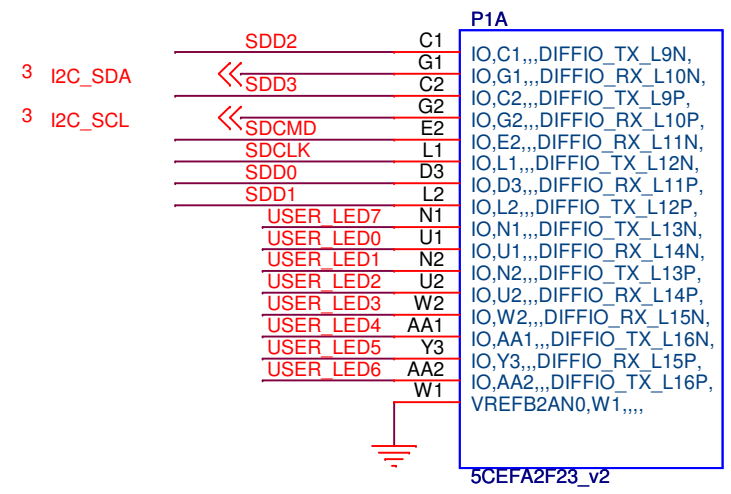
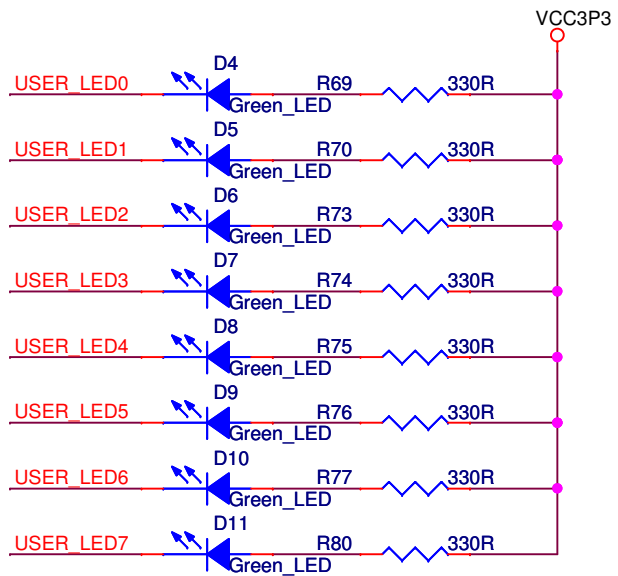
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Date:	Monday, May 06, 2013	Sheet 3 of 7



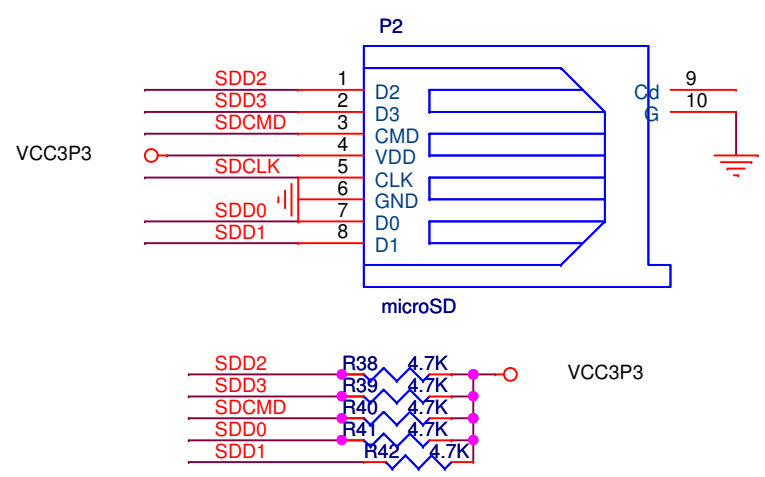
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Size	Document Number	Rev
B	FPGA Power	<RevCode>
Date:	Thursday, April 25, 2013	Sheet 4 of 7



Title		<Title>	Rev	<RevCode>
Size	Document Number	USB-Blaster		
Date:	Monday, May 06, 2013	Sheet	5 of 7	

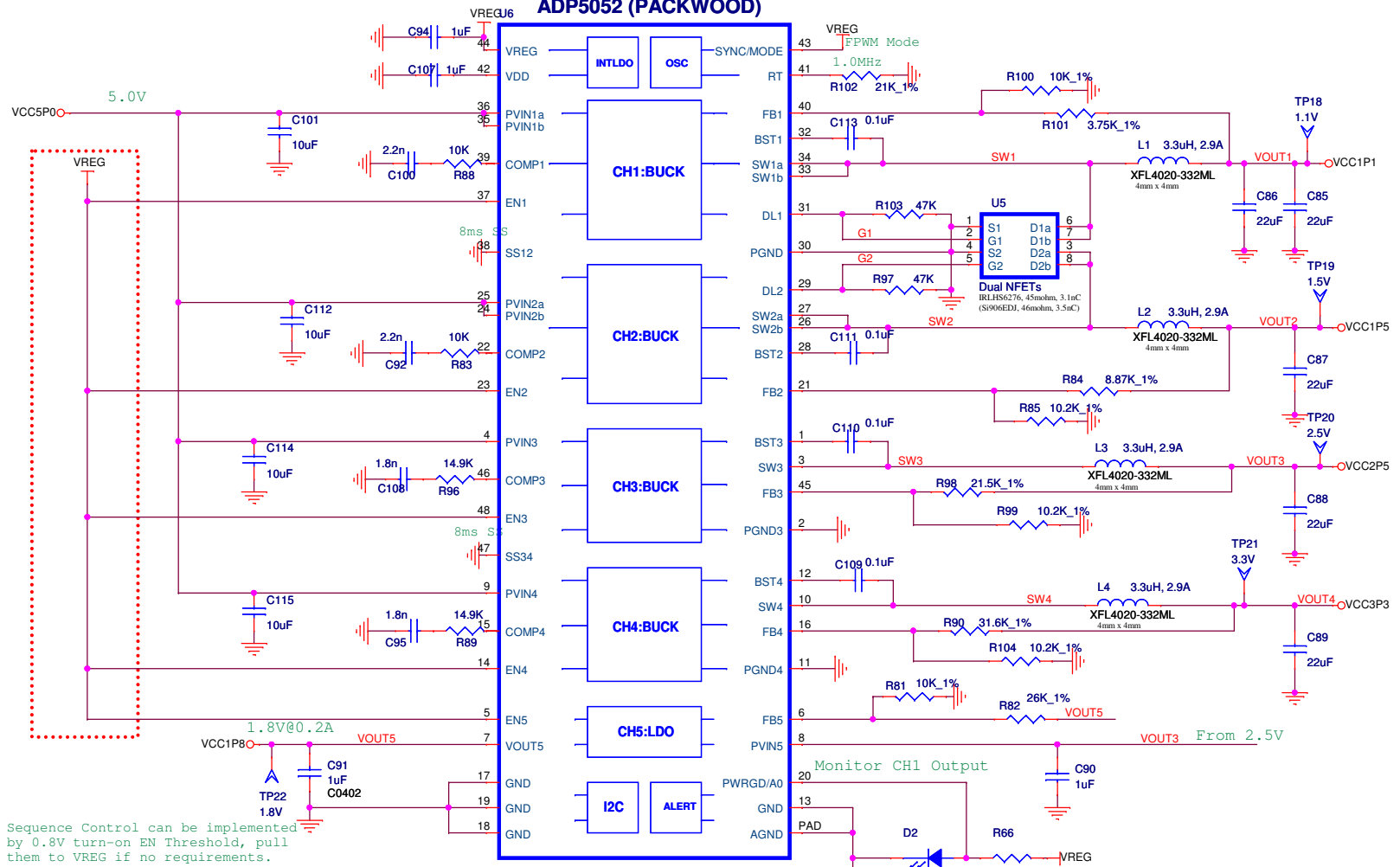


microSD



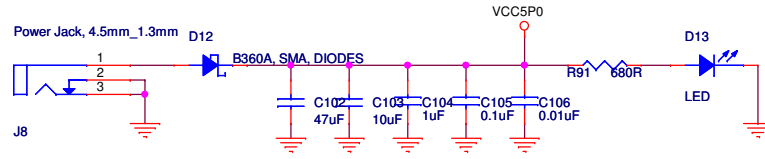
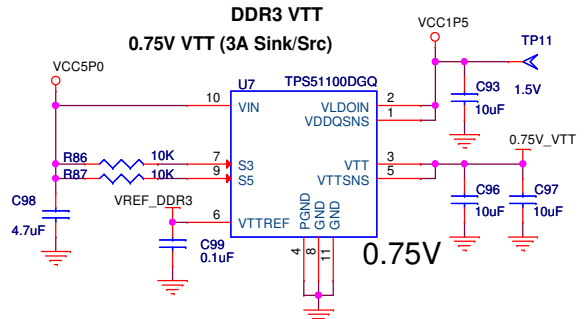
Title		
<Title>		
Size	Document Number	Rev
A	LED, EEPROM	<RevCode>
Date:	Thursday, April 25, 2013	Sheet 6 of 7

ADP5052 (PACKWOOD)



Sequence Control can be implemented by 0.8V turn-on EN Threshold, pull them to VREG if no requirements.

CAD Note:
Place caps & res near regulator
Place U38 at the same side as DDR3 addr/ctrl/cmd termination resistor packs and capacitor arrays
Pour copper on outer layer to cover these components



Title		<Title>
Size	Document Number	Rev
B	Power	<RevCode>
Date:	Thursday, April 25, 2013	Sheet 7 of 7